

FIG. 2

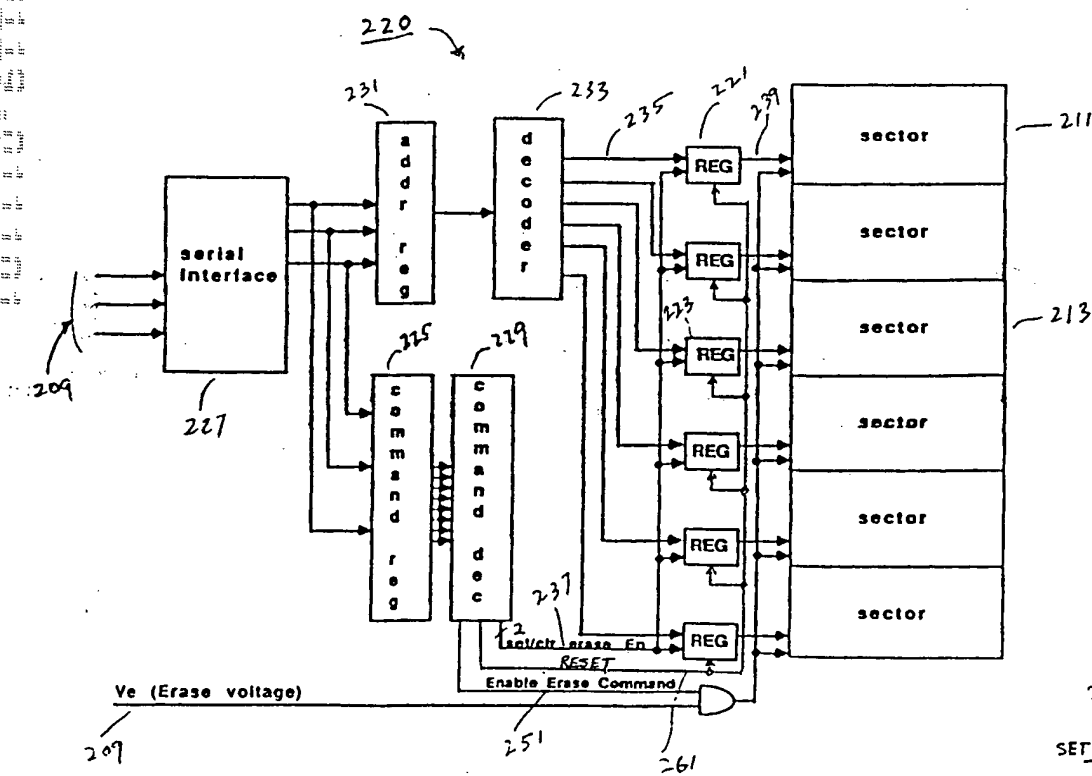


FIG. 3A

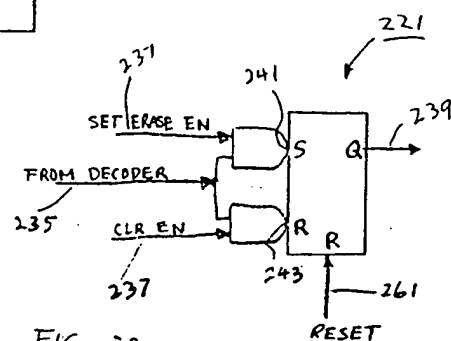


FIG. 3B

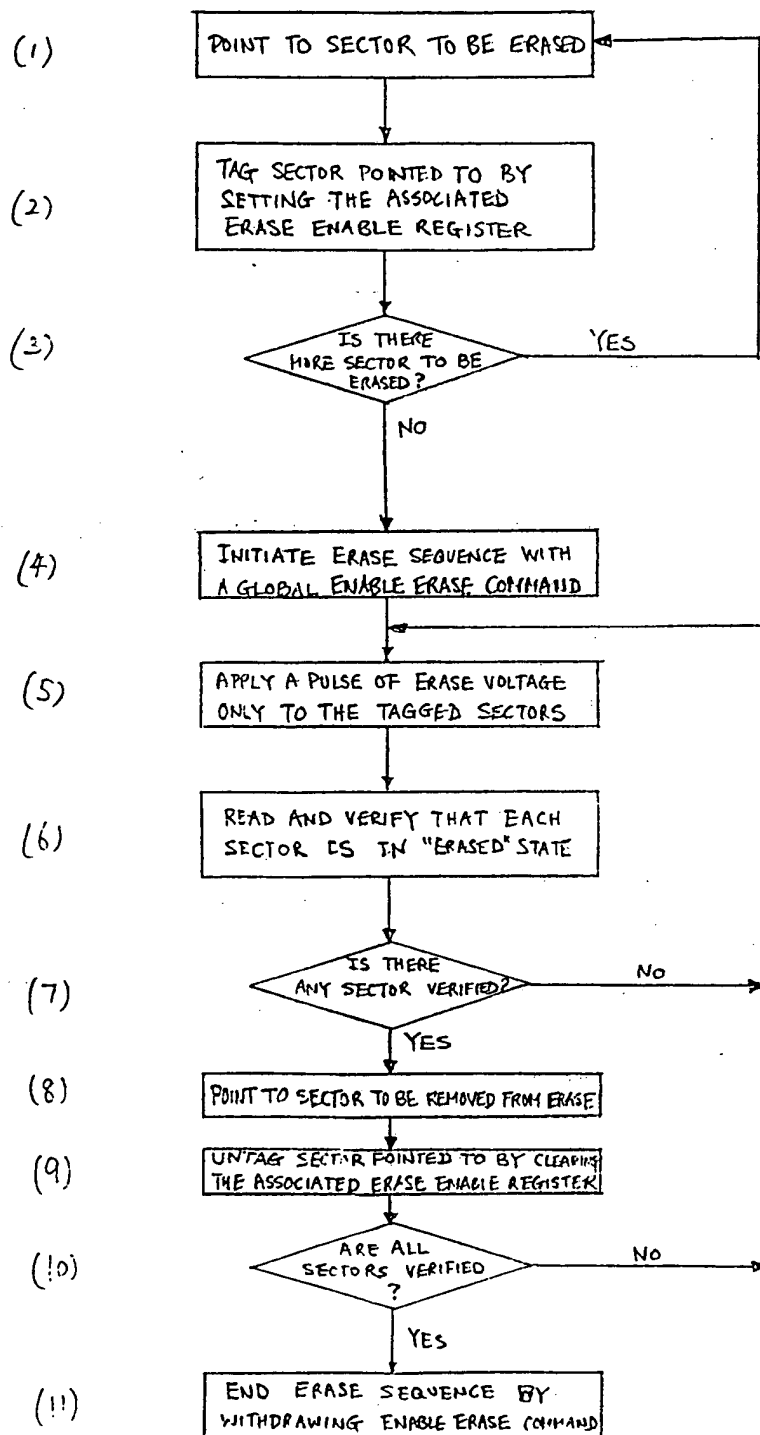
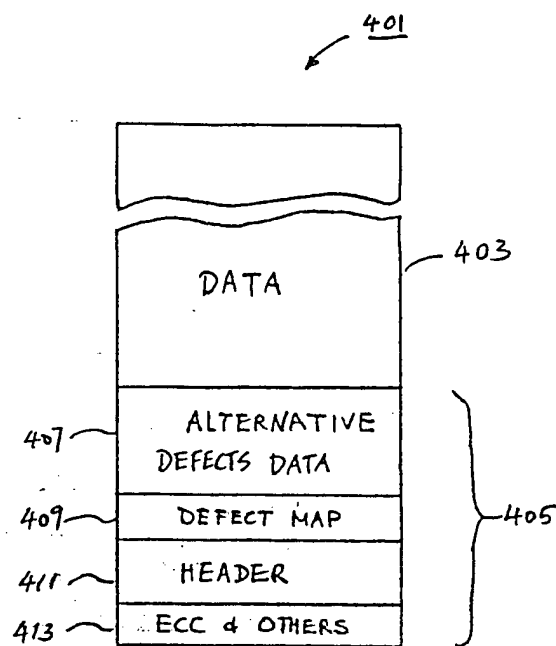


FIG - 4



SECTOR PARTITION

FIG-5

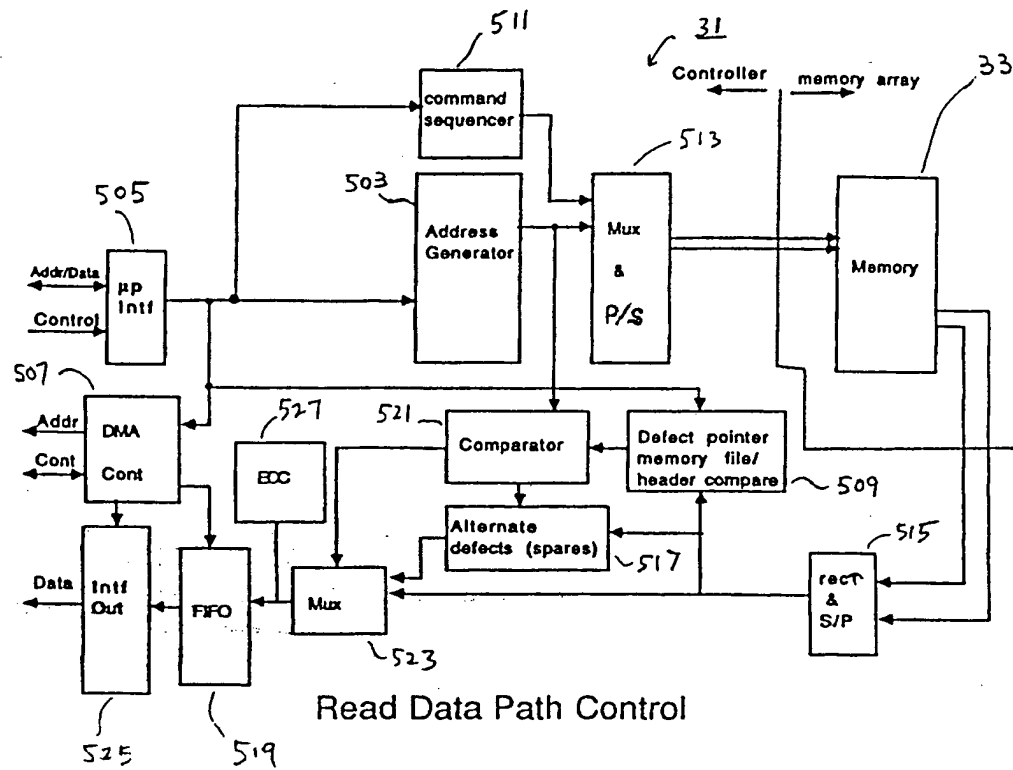


FIG. 6

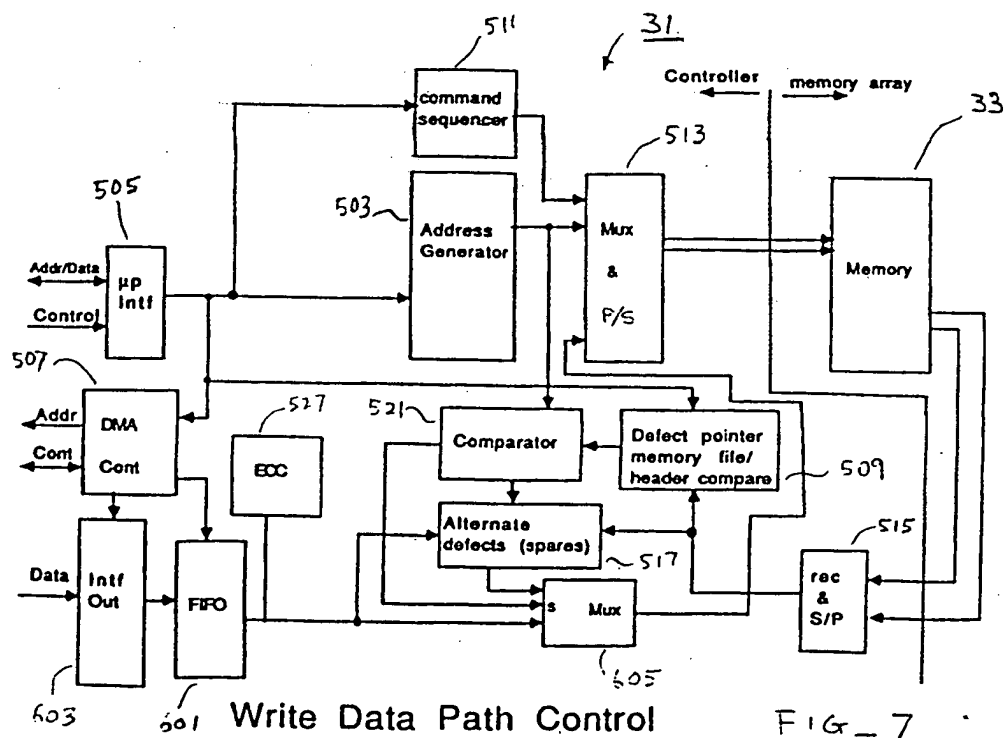


FIG. 7

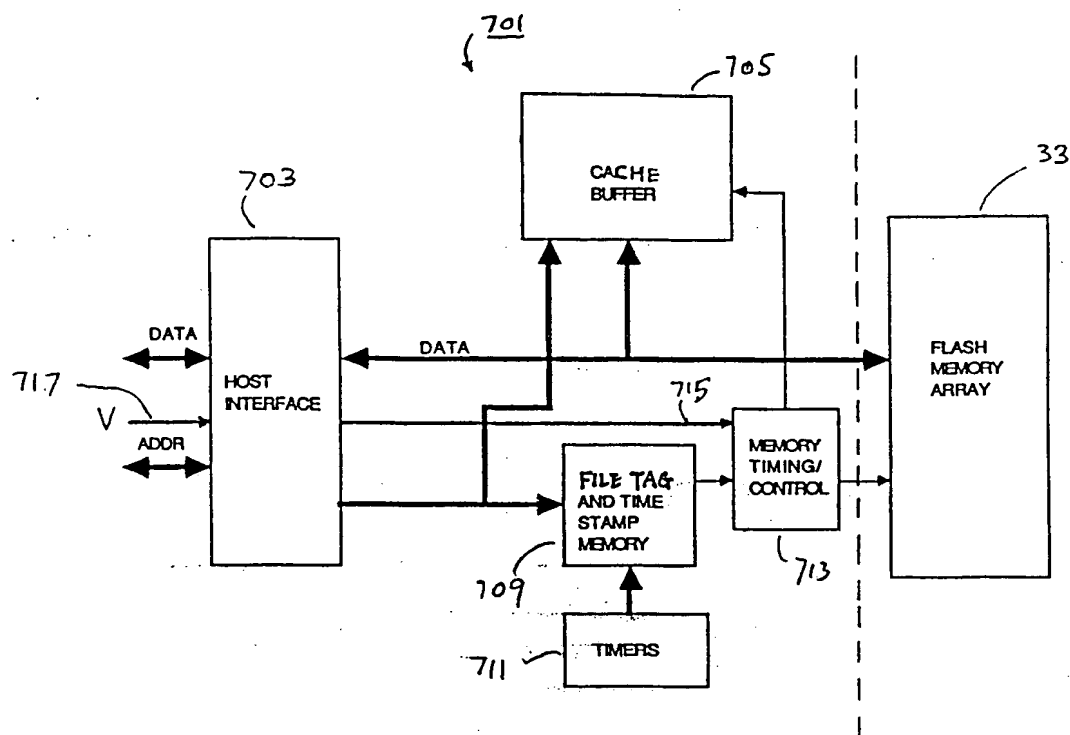


FIG. 8

7/23

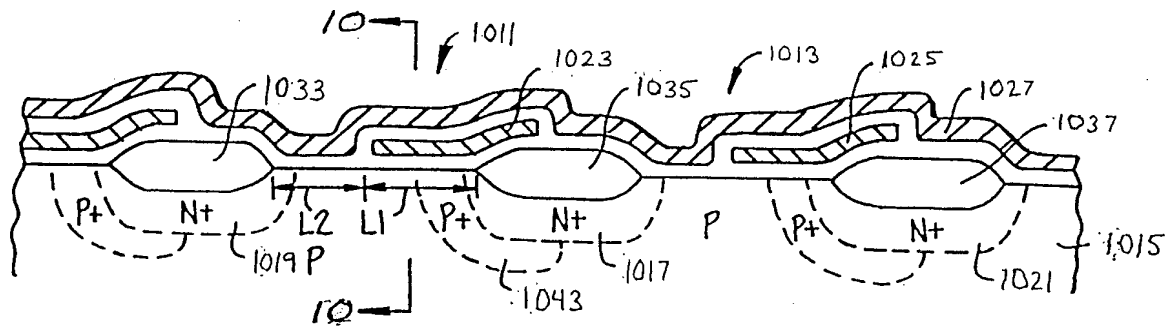


FIG. 9

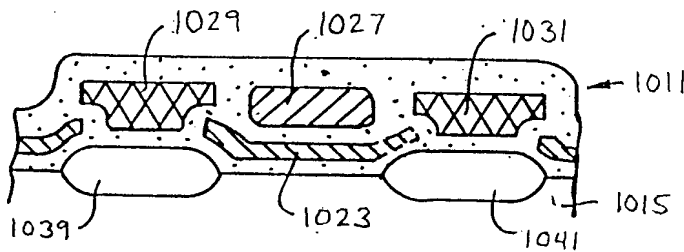


FIG. 10

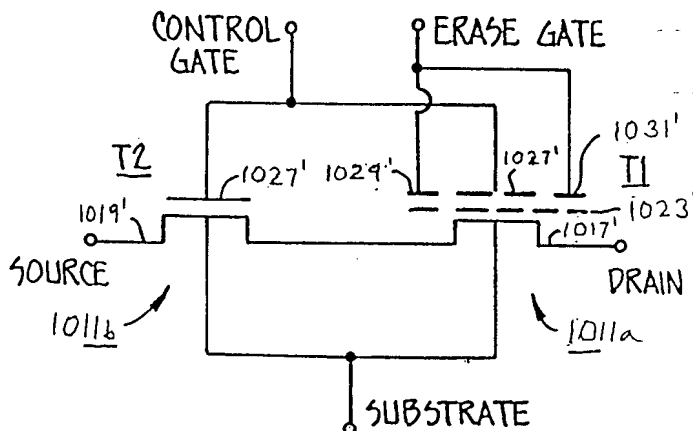


FIG. 11

8/23

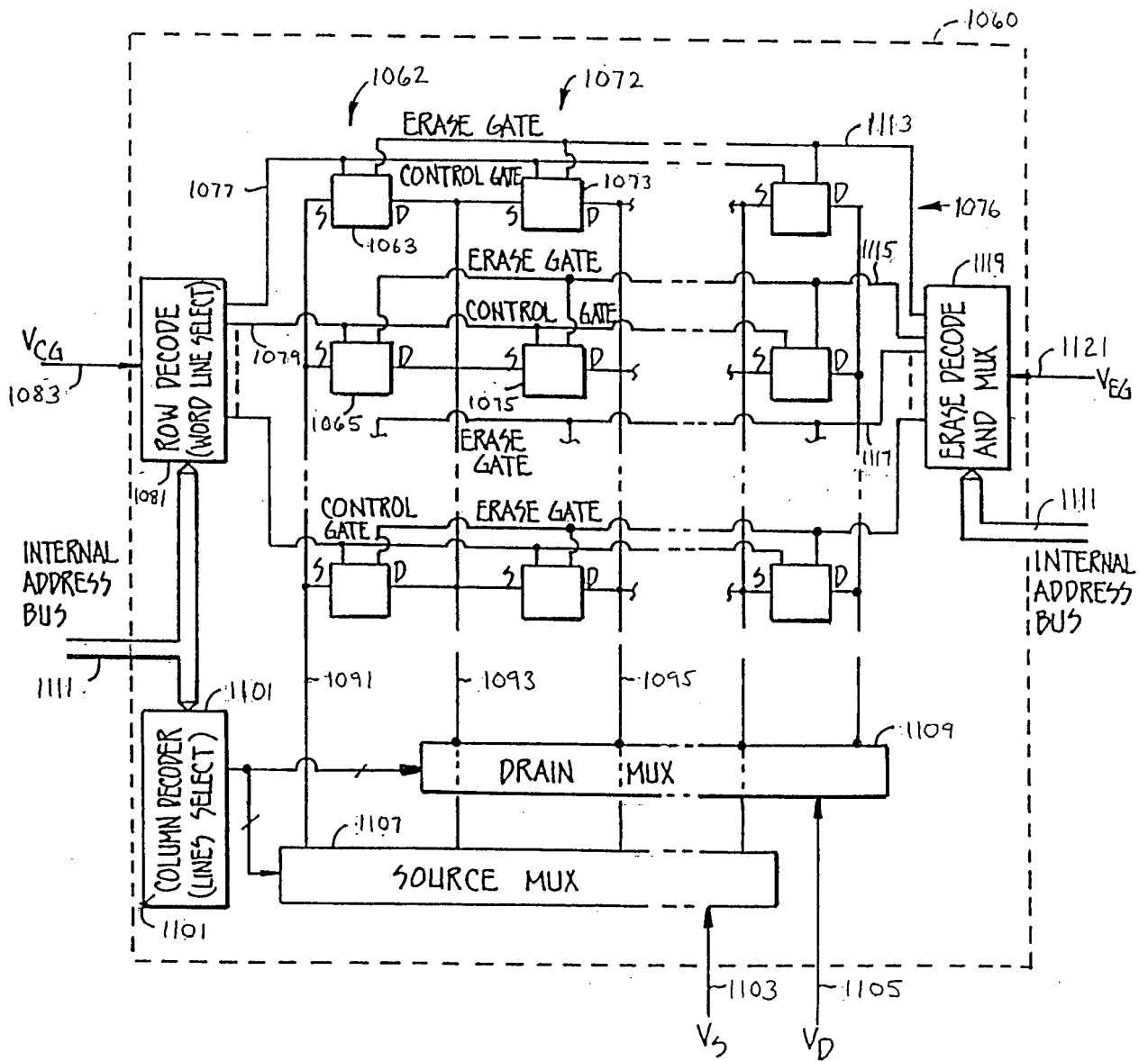


FIG. 12.

9/23

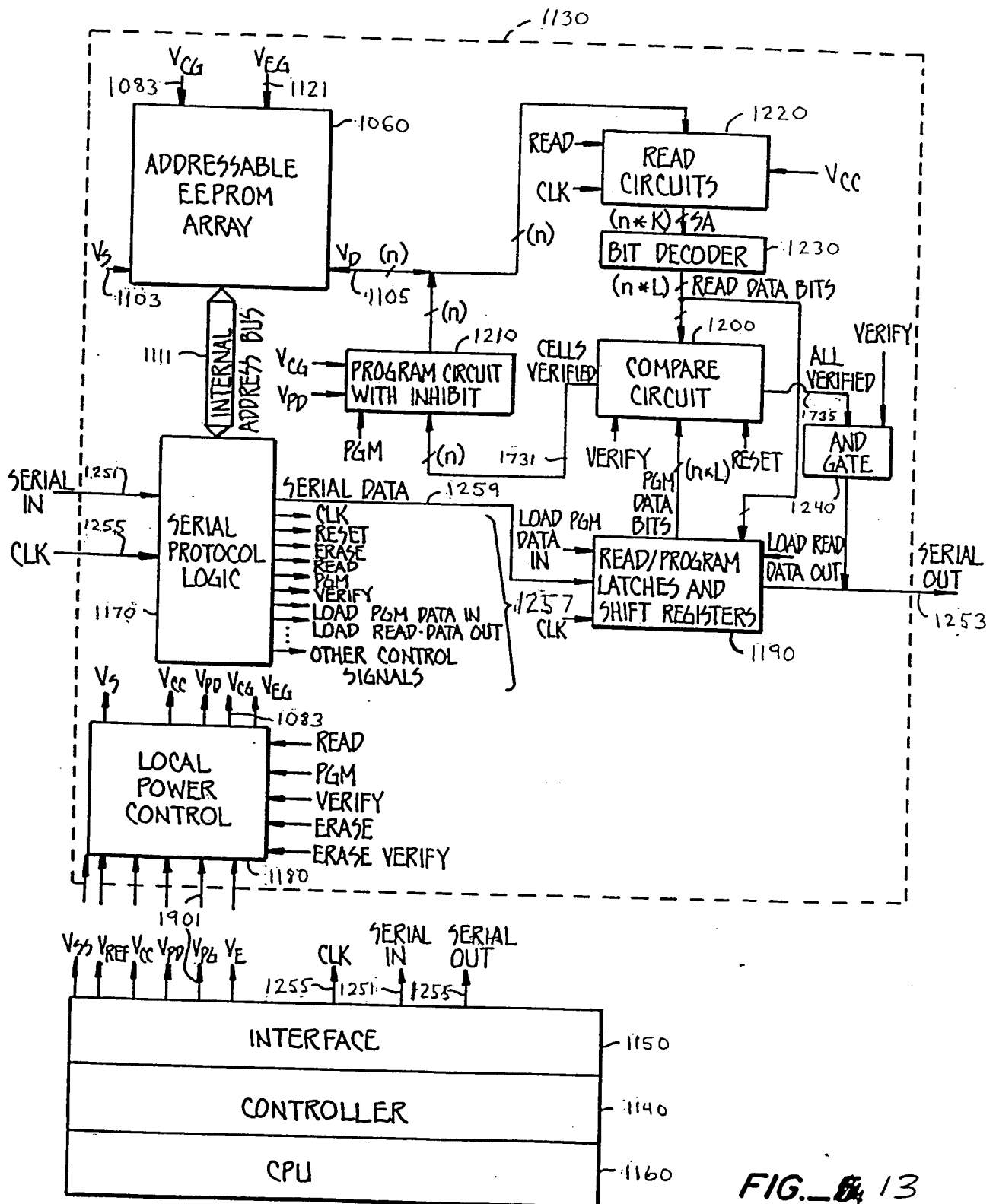


FIG. 13

10/23

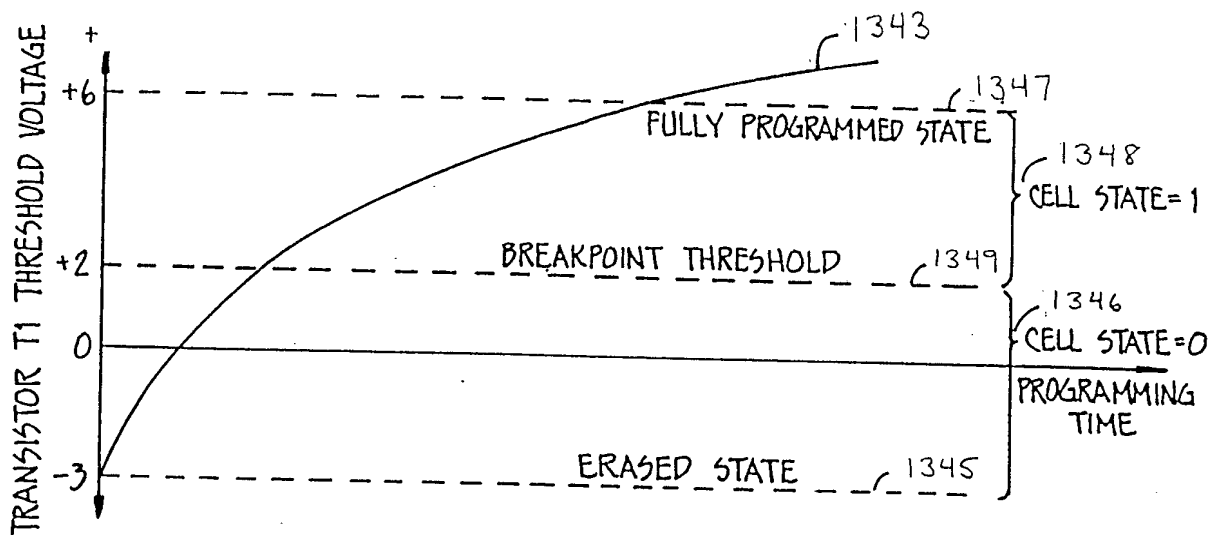


FIG. 14.

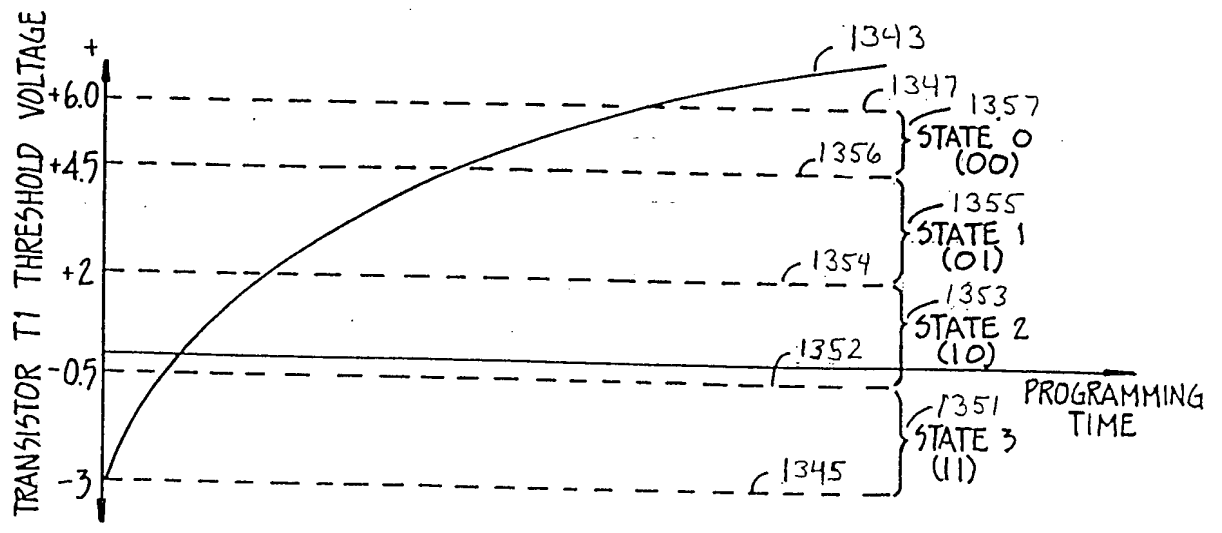


FIG. 15A

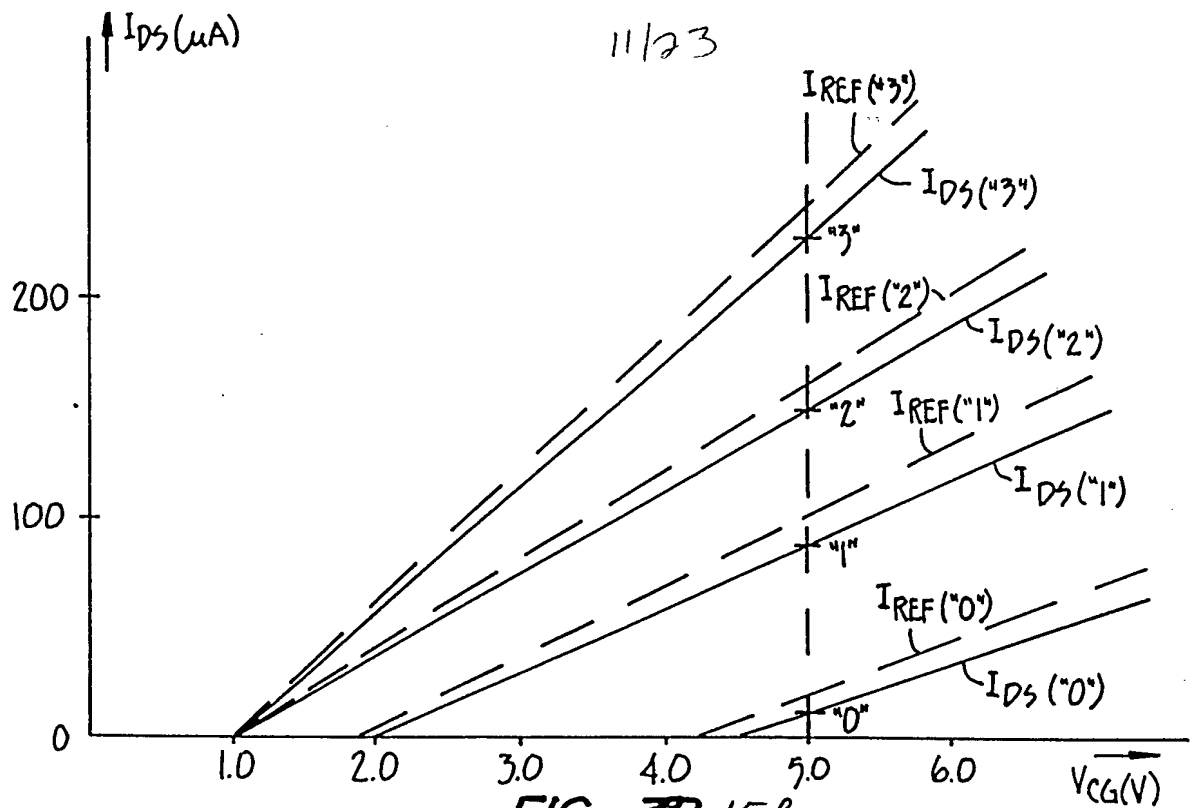


FIG. ~~7B~~ 15B

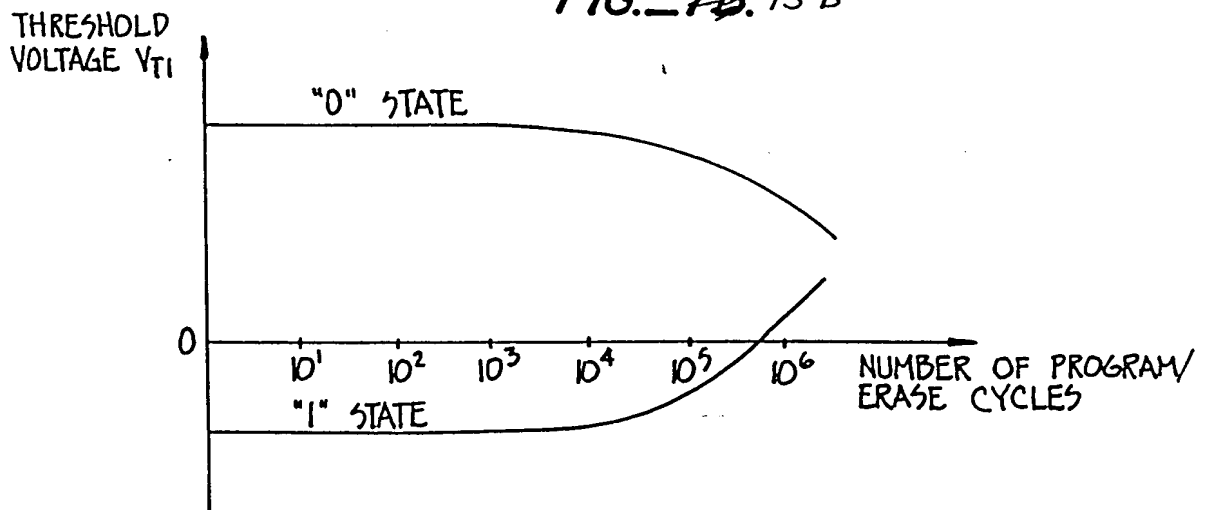


FIG. ~~8A~~ 16A

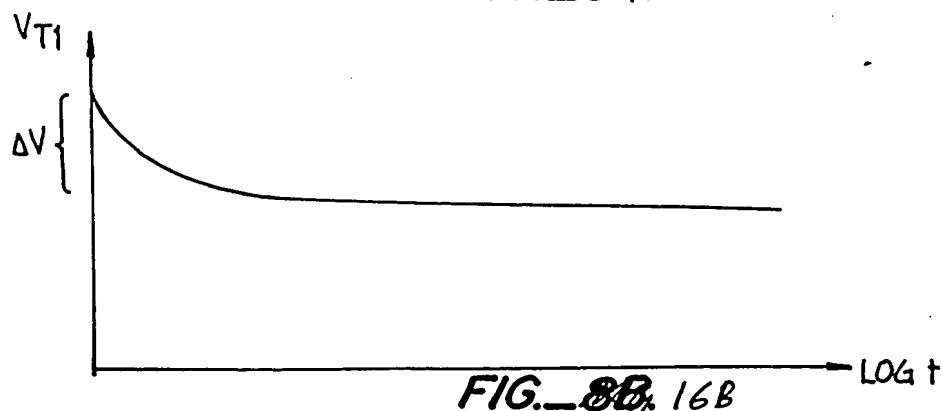


FIG. ~~8B~~ 16B

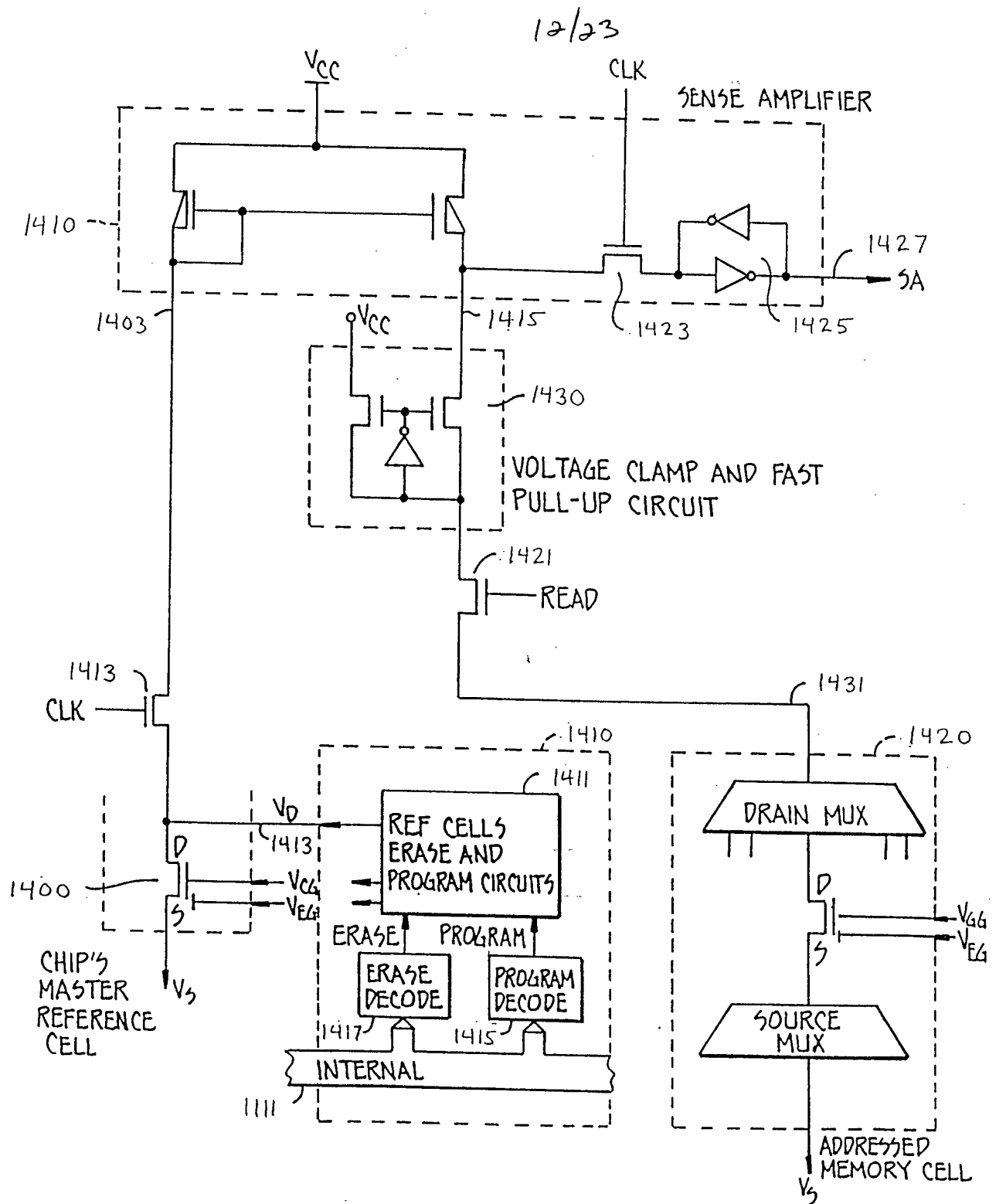


FIG. 17A

13/23

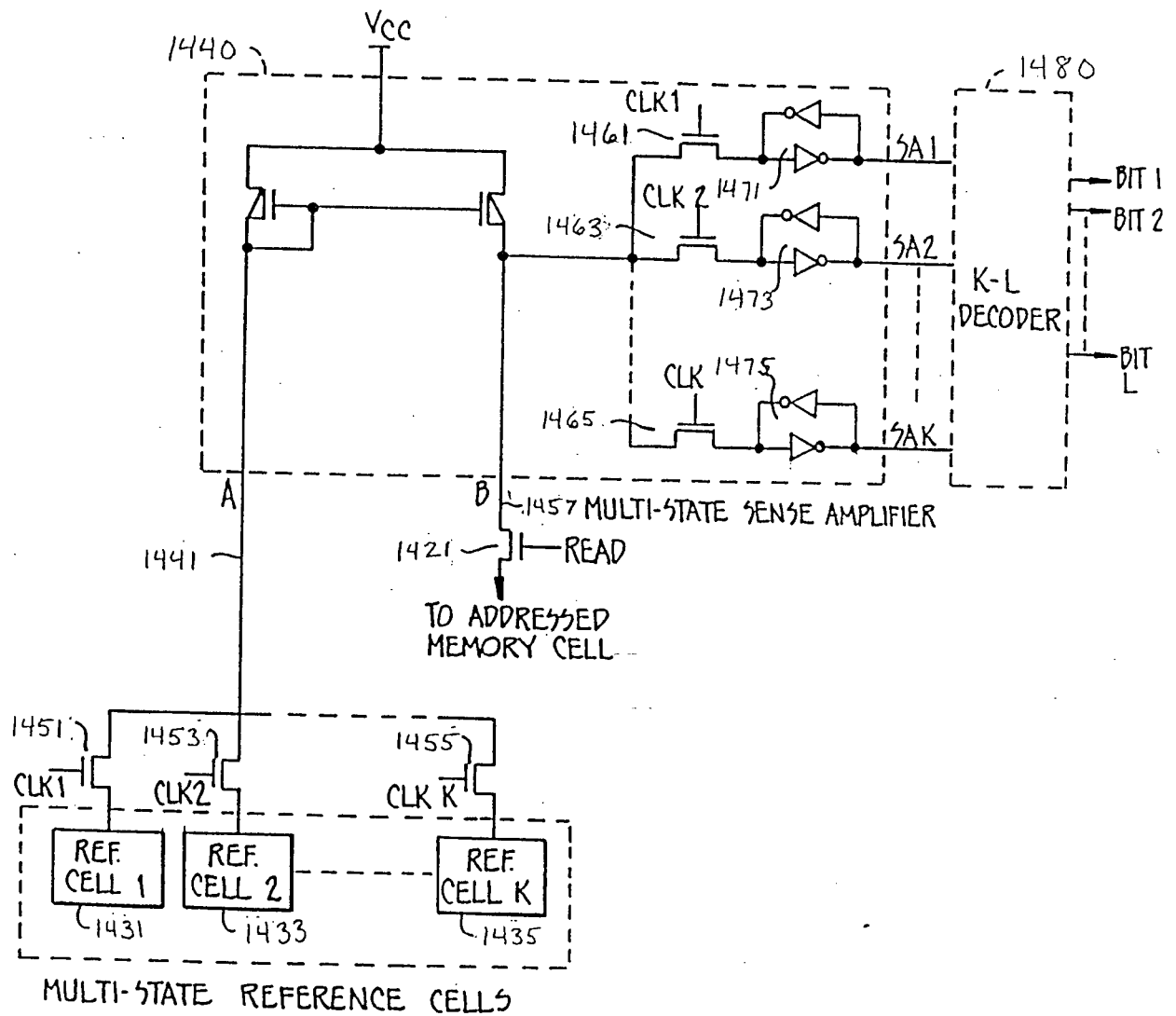


FIG. 17B

14/23

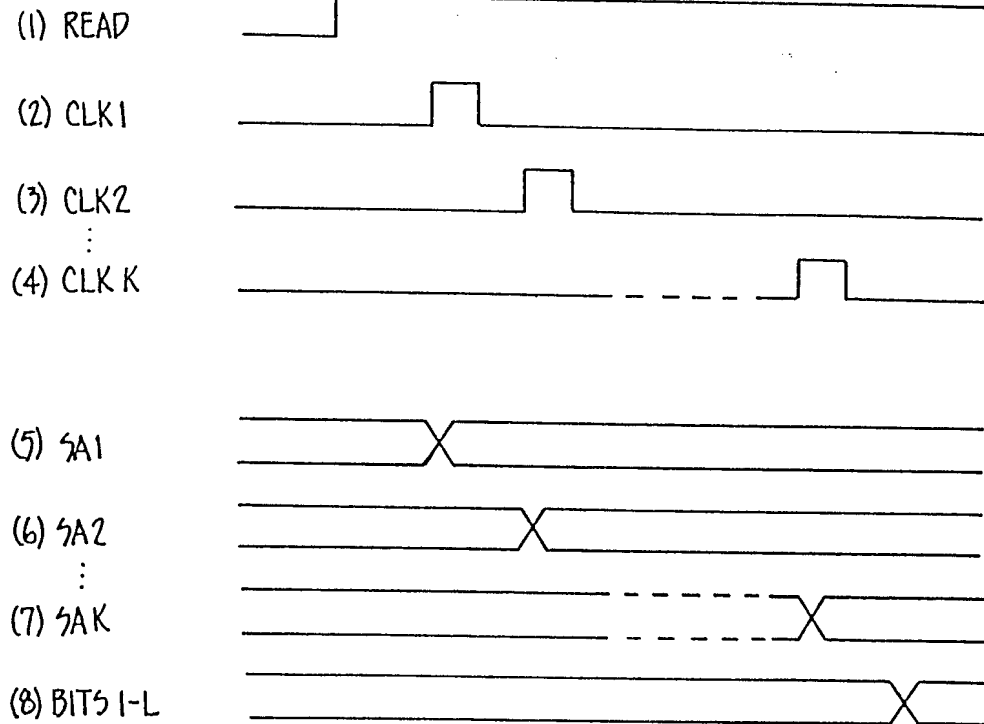


FIG. ~~10~~ 17C

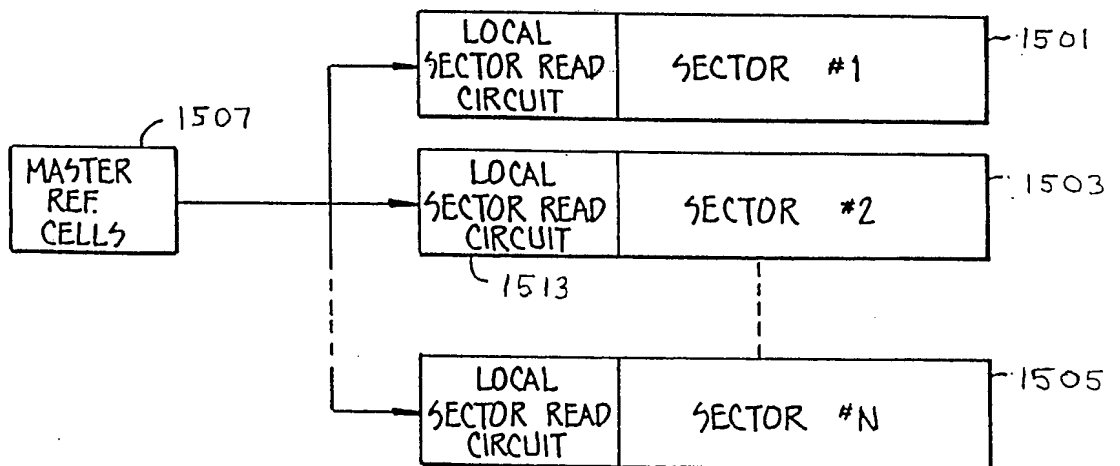


FIG. ~~10~~ 18

15/23

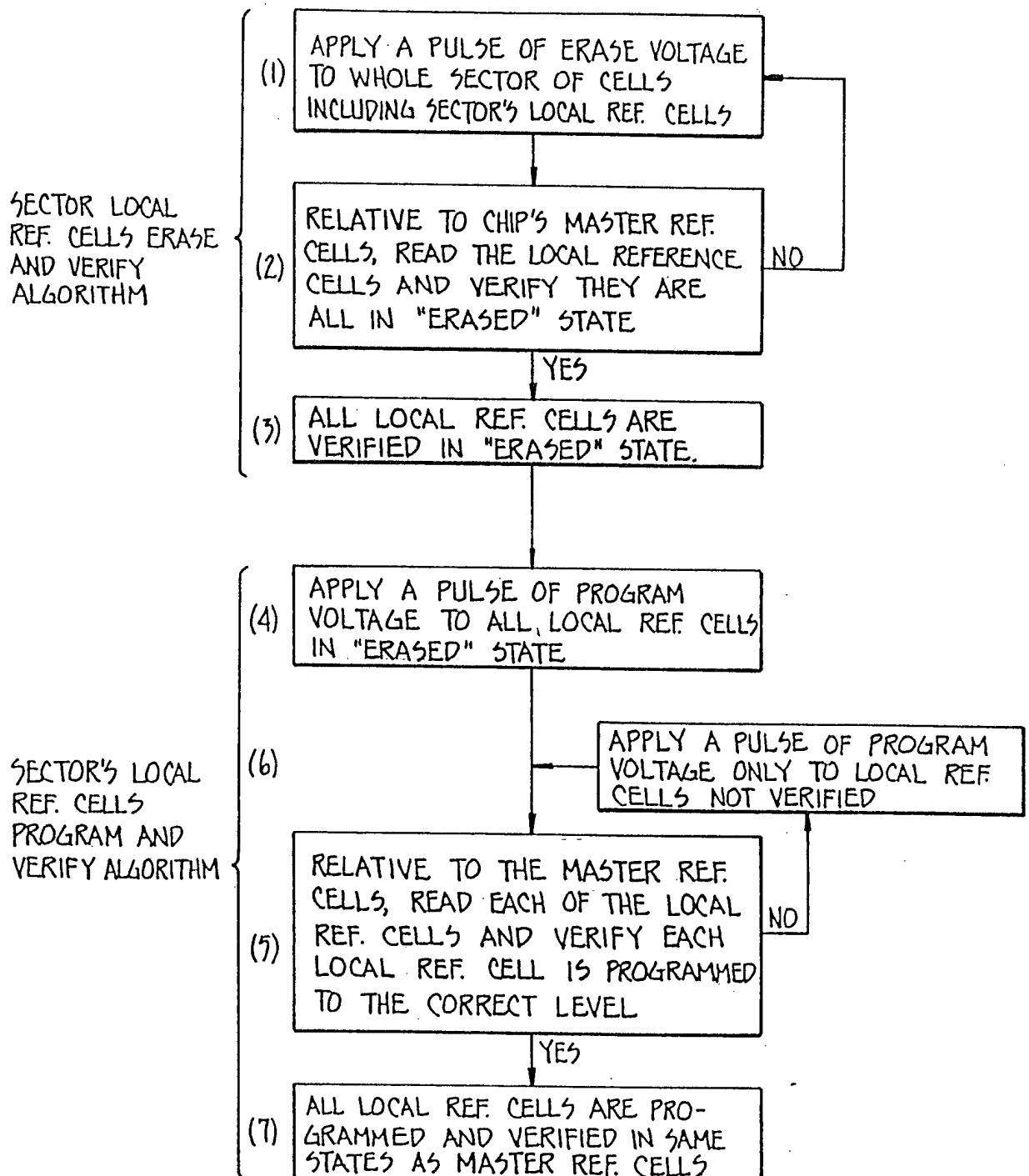


FIG. 19

\_\_\_\_\_

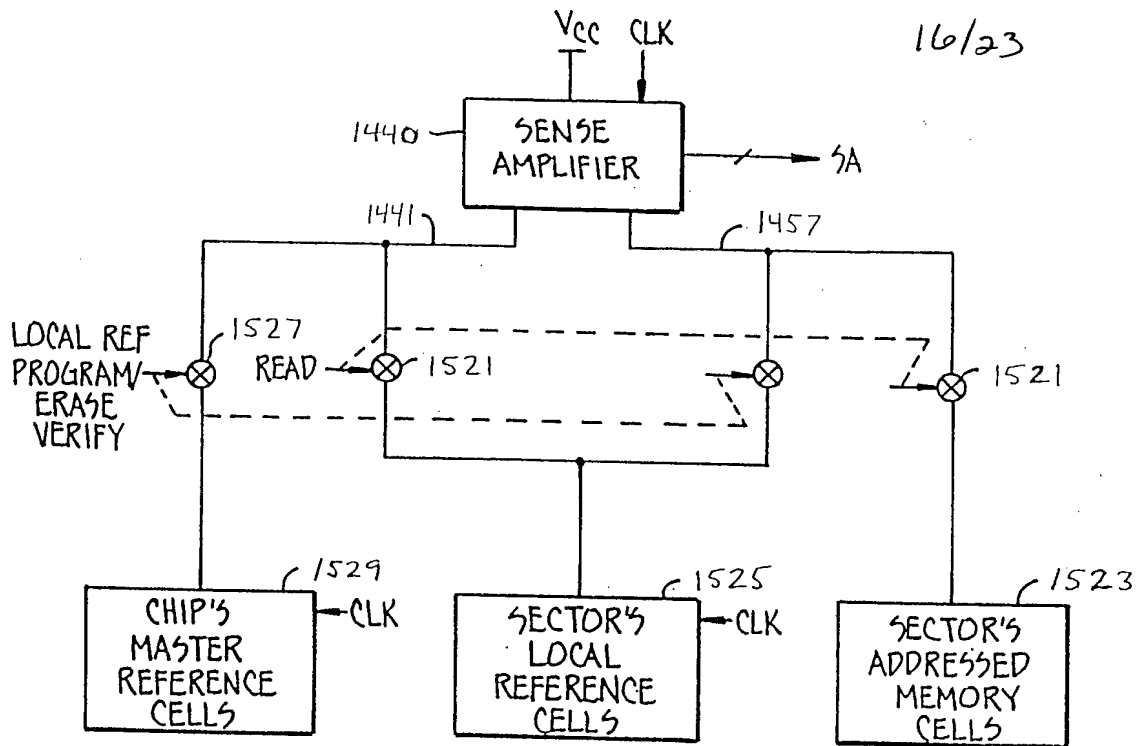


FIG. ~~2A~~ 20A

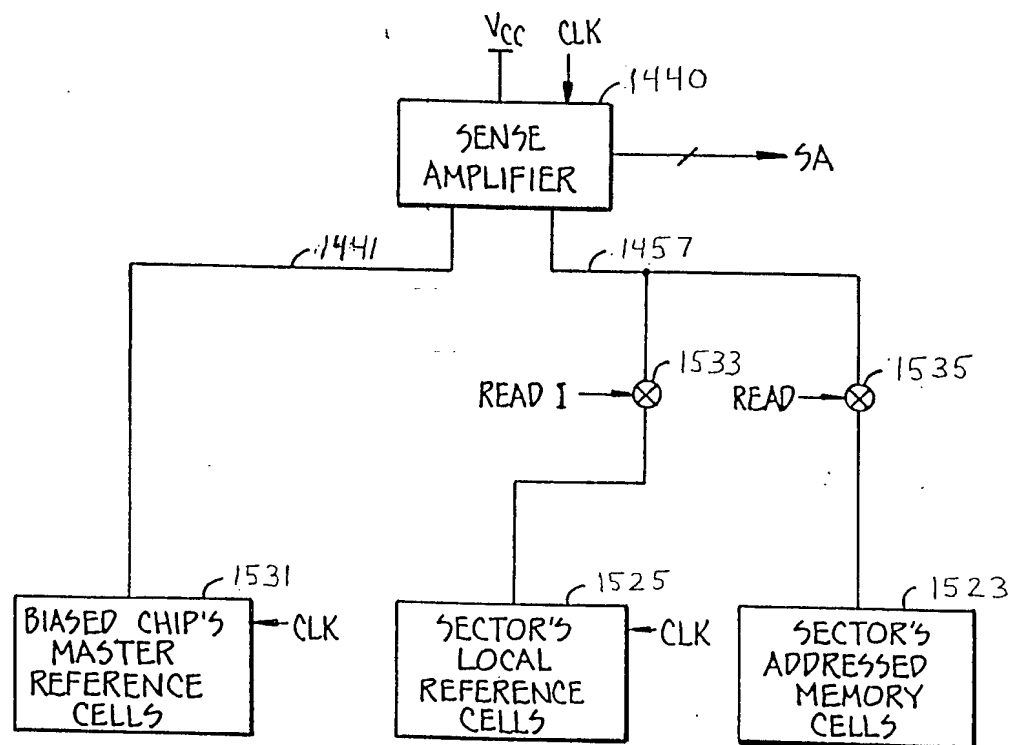


FIG. ~~13A~~ 21A

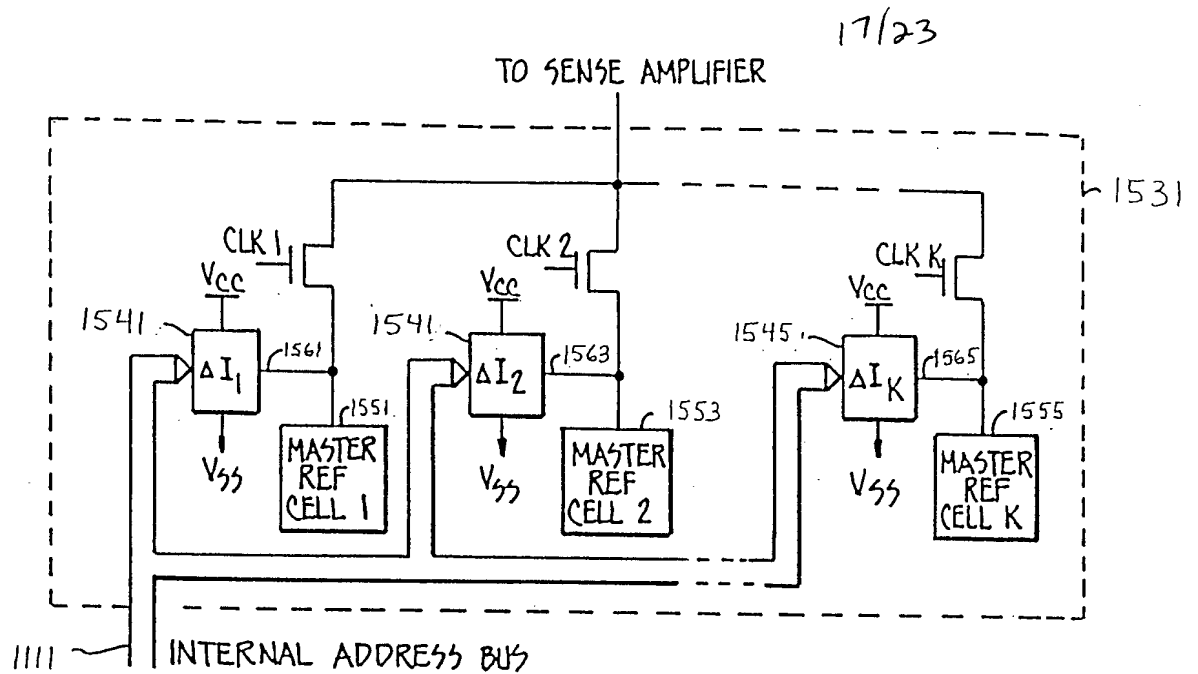


FIG. ~~13B~~ 21B

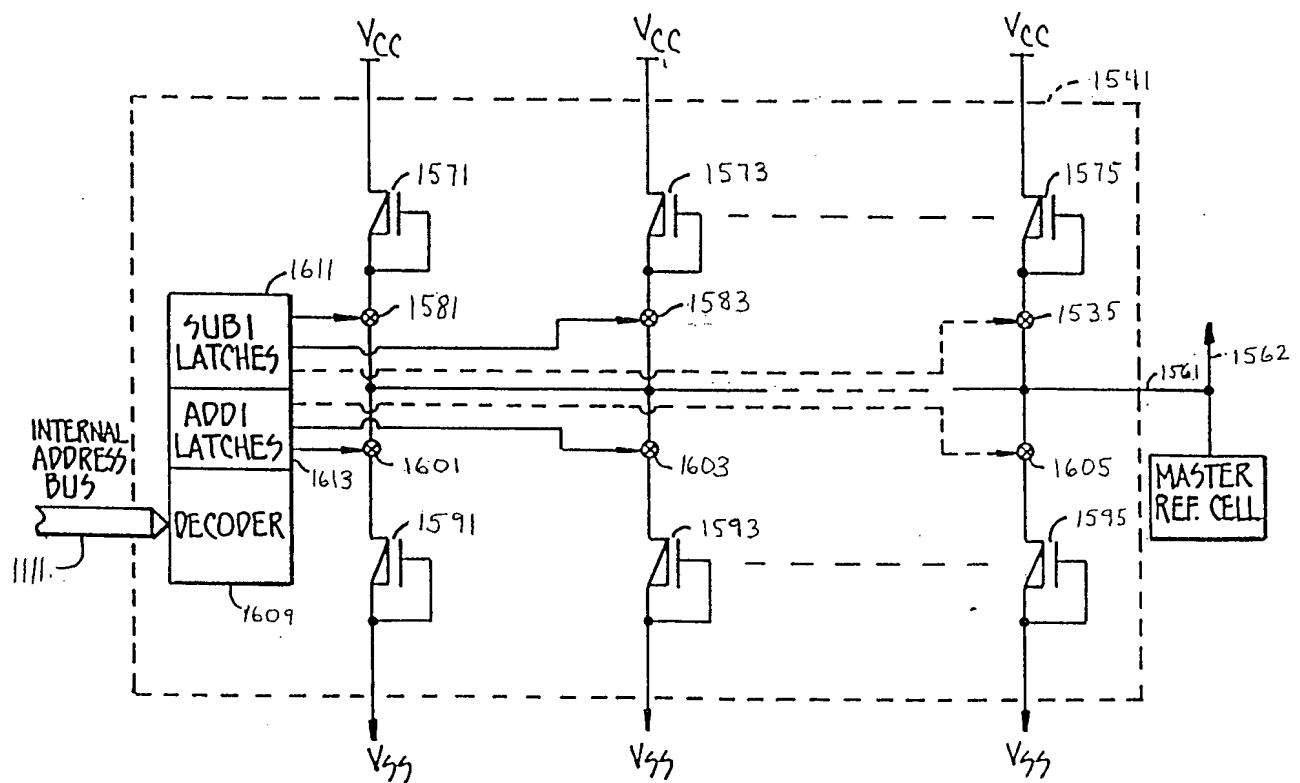


FIG. ~~13C~~ 21C

18/23

LOCAL REF. CELLS ARE PREVIOUSLY PROGRAMMED  
AND VERIFIED IN SAME STATES AS MASTER REF. CELLS

RELATIVE TO THE LOCAL REF. CELLS,  
READ THE ADDRESSED CELLS

FIG. ~~12B~~, 20B

(1)

LOCAL REF. CELLS ARE PREVIOUSLY  
PROGRAMMED AND VERIFIED IN SAME  
STATES AS MASTER REF. CELLS

(2)

RELATIVE TO THE LOCAL REFERENCE  
CELLS READ THE MASTER REF. CELLS

(3)

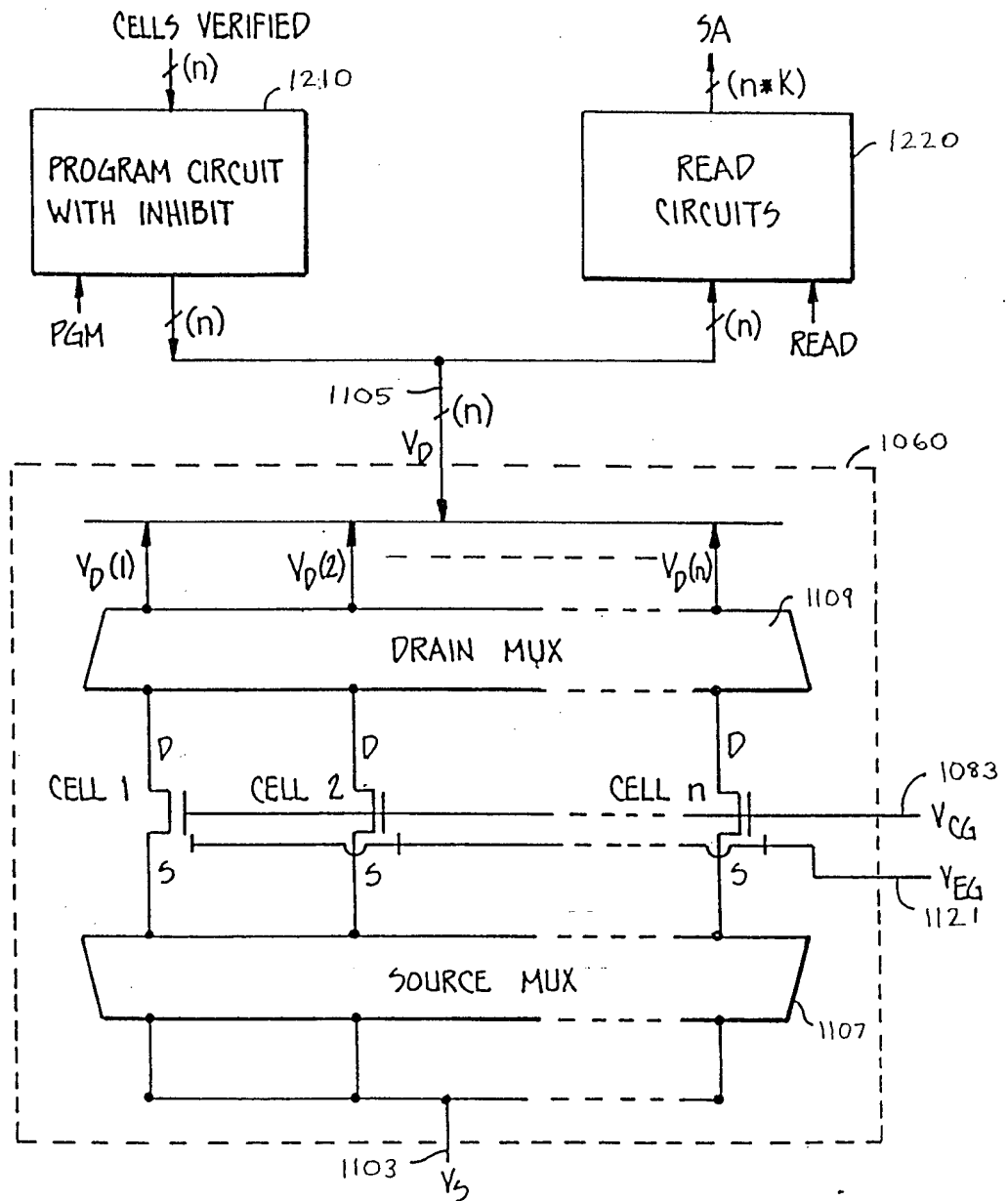
DETERMINE THE DIFFERENCES, IF ANY  
AND BIAS. THE MASTER REF CELLS'  
CURRENTS SUCH THAT THE SAME  
READING IS OBTAINED RELATIVE TO  
THE BIASED MASTER REF. CELLS  
AS RELATIVE TO THE LOCAL  
REF. CELLS

(4)

RELATIVE TO THE BIASED MASTER  
REF. CELLS, READ THE ADDRESSED CELLS

FIG. ~~13D~~, 21D

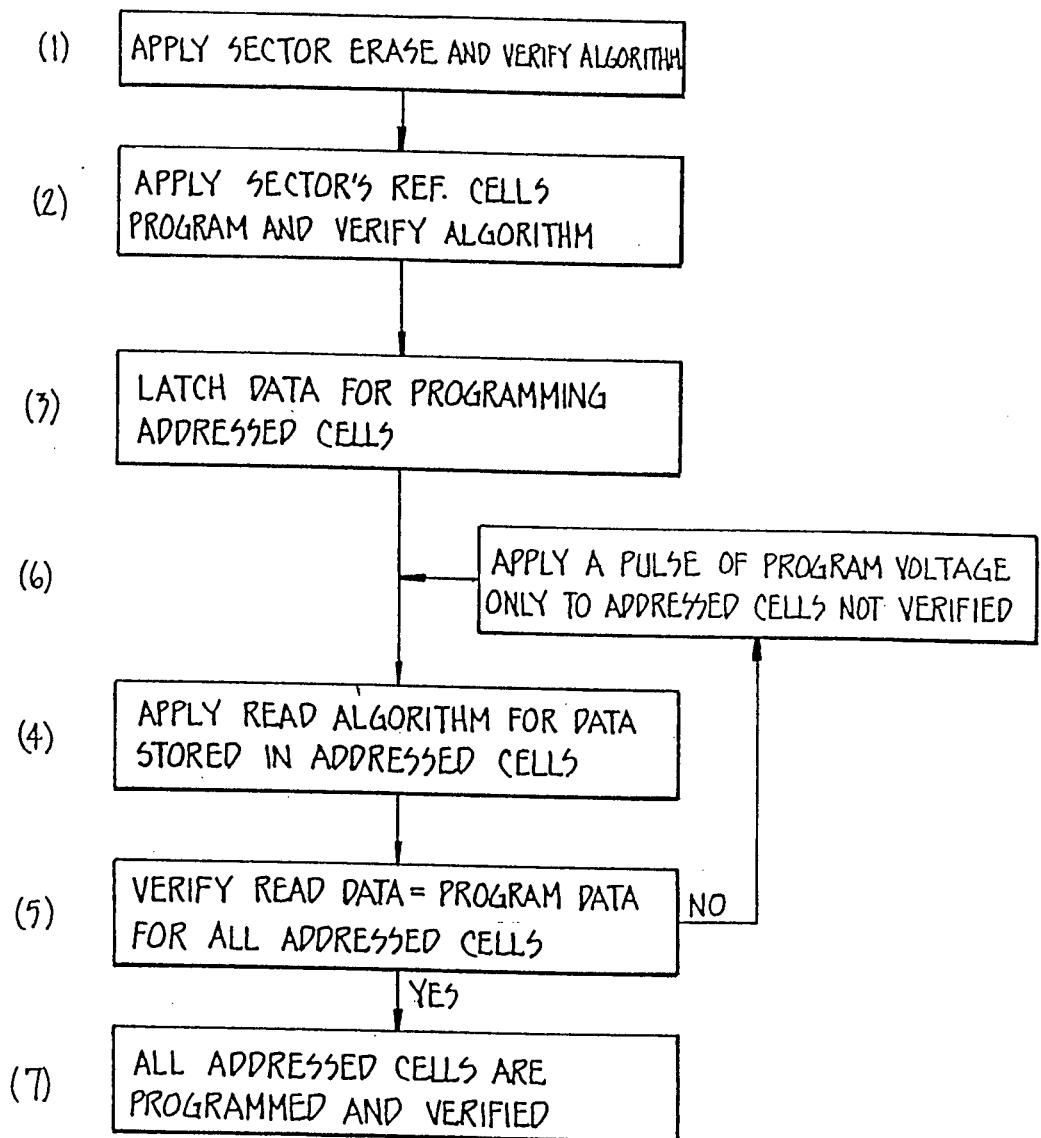
19/23



READ/PROGRAM DATA PATHS FOR n CELLS IN PARALLEL

FIG. 22.

20/23



PROGRAM ALGORITHM

FIG. 23

21/23

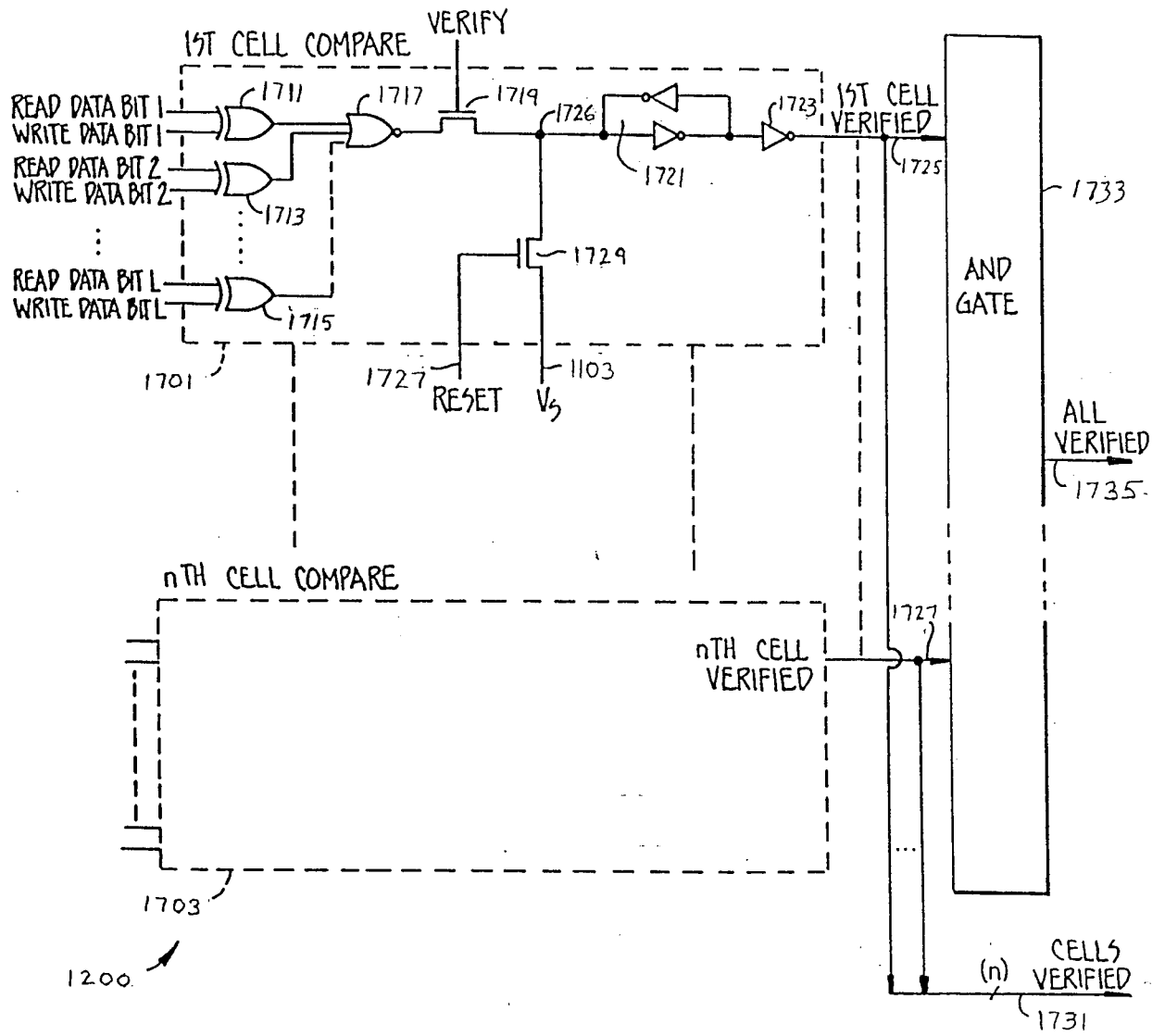


FIG. 16. 24

22/23

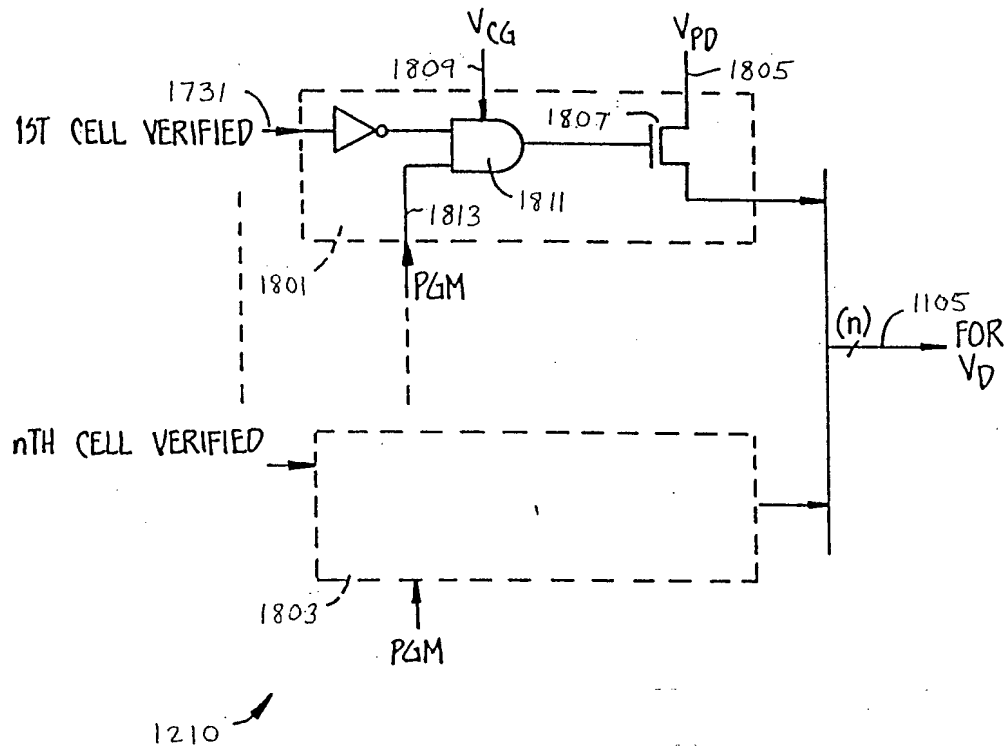


FIG. 25

23/23

	SELECTED CONTROL GATE $V_{CG}$	DRAIN $V_D$	SOURCE $V_S$	ERASE GATE $V_{EG}$
READ	$V_{PG}$	$V_{REF}$	$V_{SS}$	$V_E$
PROGRAM	$V_{PG}$	$V_{PD}$	$V_{SS}$	$V_E$
PROGRAM VERIFY	$V_{PG}$	$V_{REF}$	$V_{SS}$	$V_E$
ERASE	$V_{PG}$	$V_{REF}$	$V_{SS}$	$V_E$
ERASE VERIFY	$V_{PG}$	$V_{REF}$	$V_{SS}$	$V_E$

~~TABLE 1~~ FIG. 26

(typical values)	READ	PROGRAM	PROGRAM VERIFY	ERASE	ERASE VERIFY
$V_{PG}$	$V_{CC}$	12V	$V_{CC} + \delta V$	$V_{CC}$	$V_{CC} - \delta V$
$V_{CC}$	5V	5V	5V	5V	5V
$V_{PD}$	$V_{SS}$	8V	8V	$V_{SS}$	$V_{SS}$
$V_E$	$V_{SS}$	$V_{SS}$	$V_{SS}$	20V	$V_{SS}$
unselected control gate	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$
unselected bit line	$V_{REF}$	$V_{REF}$	$V_{REF}$	$V_{REF}$	$V_{REF}$

$V_{SS}=0V$ ,  $V_{REF}=1.5V$ ,  $\delta V=0.5V - 1V$

~~TABLE 2~~ FIG. 27